SPECIFICATION

[Title of the invention]

METHOD OF DRIVING LIQUID CRYSTAL DISPLAY

[Brief description of the drawings]

Fig. 1 is a schematic block diagram showing a configuration of a conventional liquid crystal display.

Fig. 2 shows driving waveforms of the gate driver in Fig. 1.

Fig. 3 shows gate lines supplied with the gate output enable signals in Fig. 2.

Fig. 4 depicts a process of displaying a picture on the liquid crystal display panel shown in Fig. 1.

Fig. 5A and Fig. 5B depict a process of displaying a moving picture on the liquid crystal display panel shown in Fig. 1.

Fig. 6 is an equivalent circuit diagram of the liquid crystal display panel shown in Fig. 1.

Fig. 7 is a waveform diagram of a data pulse applied to the liquid crystal cell shown in Fig. 6.

Fig. 8 shows driving waveforms of a gate driver according to a first embodiment of the present invention.

Fig. 9 shows other example of the driving waveforms.

Fig. 10 depicts a process of displaying a picture on the liquid crystal display panel by the driving waveforms shown in Fig. 8 and Fig. 9.

Fig. 11 shows driving waveforms of a gate driver according to a second embodiment of the present invention.

<Detailed description of the reference numerals>

2, 24 : a liquid crystal display panel

4 : a data driver

6 : a gate driver

16, 40 : a current frame

18, 46 : a previous frame

20, 22 : a moving picture

42 : a black picture

[Detailed description of the invention]

[Object of the invention]

[Technical field including the invention and prior art therein]

This invention relates to a technique of driving a liquid crystal display, and more particularly to a method of driving a liquid crystal display that is adaptive for improving a picture quality.

Generally, an active matrix liquid crystal display (LCD) controls a light transmissivity of a liquid crystal using an electric field applied to the liquid crystal. To this end, as shown in Fig. 1, the active matrix LCD includes a liquid crystal display panel 2 having liquid crystal cells arranged between two sheets of transparent substrates in a matrix type, a gate driver 6 connected to gate lines GL1 to GLm of the liquid crystal display panel 2, and a data driver 4 connected to data lines DL1 to DLn of the liquid crystal display panel 2.

The gate driver 6 sequentially applies a scanning pulse to m gate lines GL1 to GLm to drive a thin film transistor (TFT) connected to the corresponding gate line. The data driver 4 is synchronized with the scanning pulse sequentially applied to the gate lines GL1 to GLm to thereby supply a data corresponding to a brightness value of a video data to n data lines DL1 to DLn.

More specifically, the conventional LCD sequentially turns on or off all the gate lines GL1 to GLm provided at the liquid crystal display panel 2 during one frame and supplies a data corresponding to the turned-on gate lines GL1 to GLm to the data lines DL1 to DLn, thereby displaying a picture.

Fig. 2 shows driving waveforms of the conventional gate driver and the conventional data driver.

Referring to Fig. 2, the gate driver 6 receives a

clock signal (e.g. 22μs in the case of XGA) and a gate output enable (GOE) signal from a supplier (not shown). The gate driver 6 supplied with the clock signal and the GOE signal is synchronized with the clock signal to sequentially apply a scanning pulse SP to the 1st to mth gate lines GL1 to GLm. The data driver 4 is synchronized with the scanning pulse SP sequentially applied to the gate lines GL1 to GLm to apply a picture data D to the data lines DL1 to DLn.

Meanwhile, the GOE signal is divided into first to third GOE signals GOE1 to GOE3. As shown in Fig. 3, the first gate output enable signal GOE1 is applied to the (3i+1)th gate lines GL1, GL4, ... (wherein i is an integer). The second gate output enable signal GOE2 is applied to the (3i+2)th gate lines GL2, GL5, ... The third gate output enable signal GOE3 is applied to the (3i+3)th gate lines GL3, GL6, ...

The gate lines GL1 to GLm remains at a low state when the first to third gate output enable signals GOE1 to GOE3 have a high state. In other words, when the first gate output enable signal GOE1 has a high state, the (3i+1)th gate lines GL1, GL4, ... remains at a low state.

Such gate output enable signals GOE1 to GOE3 are utilized to prevent a crosstalk phenomenon between the adjacent pixel cells. The first gate output enable signal GOE1 maintains a high state between a scanning pulse SP applied to the (3i+1)th gate lines GL1, GL4, ... and a scanning pulse SP applied to the (3i+2)th gate lines GL2, GL5, ... In other words, the first gate output enable signal GOE1 remains at a high state before a clock signal for applying the scanning pulse SP to the (3i+2)th gate lines GL2, GL5, ... maintains a high state.

Accordingly, a time at which the scanning pulse SP applied to the (3i+1)th gate lines GL1, GL4, ... is changed into a low state is equal to a time at which the scanning pulse SP applied to the (3i+2)th gate lines GL2, GL5, ...

is changed into a high state, so that it becomes possible to prevent the crosstalk phenomenon.

Similarly, the second gate output enable signal GOE2 maintains a high state between a scanning pulse SP applied to the (3i+2)th gate lines GL2, GL5, ... and a scanning pulse SP applied to the (3i+3)th gate lines GL3, GL6, ... The third gate output enable signal GOE3 remains at a high state between a scanning pulse SP applied to the (3i+3)th gate lines GL3, GL6, ... and a scanning pulse SP applied to the (3i+1)the gate lines GL4, GL7, ...

If a scanning pulse SP is applied to the (m-10)th gate line GLm-10 by means of the gate driver 6, then the liquid crystal display panel 2 is divided into a current frame 16 and a previous frame 18 on a basis of the (m-10)th gate line GLm-10 as shown in Fig. 4. A picture to be displayed in the current frame is displayed in the current frame 16 while a picture having been displayed in the previous frame is displayed in the previous frame 18.

Accordingly, if a moving picture shifted from the right side of the liquid crystal display panel 2 into the left side thereof is displayed, then a moving picture 20 displayed in the current frame 16 and a moving picture 22 displayed in the previous frame 18 go amiss on a basis of the (m-10)th gate line GLm-10 as shown in Fig. 5A. At this time, the previous data picture overlaps with the current data picture by a portion 24 at which the moving picture 20 displayed in the current frame 16 has been shifted, as shown in Fig. 5B. When the previous data picture overlaps with the current data picture in this manner, a motion blur phenomenon is generated to deteriorate a picture quality in the liquid crystal display panel 2.

Each pixel of the liquid crystal display panel 2 can be represented with an equivalent circuit in Fig. 6. In Fig. 6, the pixel includes a TFT connected among a gate line GL, a data line DL and a common voltage line CL, and a liquid crystal cell Clc connected between a drain terminal of the

TFT and a reference voltage line. The pixel of the liquid crystal display panel 2 further includes a parasitic capacitor Cgs formed between the drain terminal of the TFT and the gate line GL, and a storage capacitor Cst positioned between the common voltage line CL and a ground voltage source GND.

As shown in Fig. 7, when a gate high voltage Ghv is applied to the gate line GL of the liquid crystal display panel 2, a data pulse is applied to the data line DL. Such a data pulse drops by a desired voltage ΔV when the gate high voltage Vhv is changed into a low state. This causes a brightness deterioration in the liquid crystal display panel 2, that is, a picture quality deterioration in the liquid crystal display panel 2. A voltage drop amount ΔV of the data pulse is determined by the following equation:

$$\Delta V_p = (C_{gs}/C_{gs}+C_{st}+C_{lc}) * (V_{gh}-V_{gl}) \quad \ldots (1)$$

wherein Clc represents a capacitor of the liquid crystal capacitor; Vgh does a gate high voltage value; and Vgl does a gate low voltage value.

In the equation (1), the parasitic capacitor Cgs, the storage capacitor Cst, the gate high voltage value Vgh and the gate low voltage value Vgl are fixed, whereas a capacitance value of the liquid crystal cell Clc is determined by a displayed picture. If a stationary picture is displayed on the liquid crystal display panel 2, then a voltage drop amount ΔV of the data pulse can be forecasted because a capacitance value of the liquid crystal cell Clc has been fixed. Thus, the voltage drop amount ΔV of the data pulse can be compensated to thereby prevent a picture quality deterioration in the liquid crystal display panel 2.

If a moving picture is displayed on the liquid crystal display panel 2, however, a voltage drop amount ΔV of the data pulse can be forecasted because a capacitance value of the liquid crystal cell Clc is varied. Thus, the voltage

drop amount ΔV of the data pulse fails to be compensated to cause a picture quality deterioration in the liquid crystal display panel 2.

[Technical Subject Matter to be solved by the Invention]

Accordingly, it is an object of the present invention to provide a method of driving a liquid crystal display that is adaptive for improving a picture quality.

[Configuration and Operation of the Invention]

In order to achieve these and other objects of the invention, a method of driving a liquid crystal display according to one aspect of the present invention includes the steps of applying a clock pulse to a gate driver; applying first to third gate output enable signals to the gate driver; and applying a scanning pulse to two gate lines during one period of the clock pulse.

These and other objects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings.

Hereinafter, the preferred embodiments of the present invention will be described in detail with reference to Figs. 8 to 10.

Fig. 8 shows driving waveforms of the gate driver according to a first embodiment of the present invention.

Referring to Fig. 8, the gate driver applies a scanning pulse SP to two gate lines GL during one period of a clock signal.

Hereinafter, an operation process will be described assuming that a scanning pulse SP should be applied to the first gate line GL1 and the 32nd gate line GL32.

First, the gate driver is synchronized with a clock signal to apply a scanning pulse SP to the first gate line GL1 and the 32nd gate line GL32. At this time, a second gate output enable signal GOE2 remains at a high state

during a half period of the clock signal (e.g., when the clock signal has a high state). Thus, the 32nd gate line supplied with the second gate output enable signal GOE2 remains at a low state during a half period of the clock signal at which the second gate output enable signal GOE2 maintains a high state. On the other hand, the first gate output enable signal GOE1 remains at a high state during a half period of the clock signal (e.g. when the clock signal has a low state). Thus, the first gate line GL1 remains at a low state during a half period of the clock signal at which the first gate output enable signal GOE1 maintains a high state. In other words, two gate lines GL alternately maintain a high state during one period of the clock signal.

The data driver supplies a picture data D to be displayed to the data lines DL when a scanning pulse SP is applied to the first gate line GL1 while supplying a reset data R corresponding to a black to the data lines DL when a scanning pulse SP is applied to the 32nd gate line GL32. In other words, the data driver sequentially supplies the picture data D and the reset data R to the data lines DL during one period of a horizontal synchronous signal Hsync. To this end, a pulse signal having twice the frequency in the prior art is applied to the data driver. Alternately, the data driver may sequentially supply the reset data R and the picture data D to the data lines DL during one period of a horizontal synchronous signal Hsync, as shown in Fig. 9.

After a scanning pulse was applied to the first gate line GL1 and the 32nd gate line GL32, a scanning pulse SP is applied to the second gate line GL2 and the 33rd gate line GL3 during one period of the next clock. The data lines DL are synchronized with the scanning pulse SP to be supplied with the picture data D and the reset data R.

More specifically, a scanning pulse SP is synchronized with a clock signal to be sequentially applied to the (3i+1)th, (3i+2)th and (3i+3)th gate lines GL. After a

scanning pulse SP was applied to the (3i+1)th gate lines GL1, GL4, ..., the scanning pulse SP is applied to the (3i+2)th gate lines GL2, GL5, ... preceded by a desired line. Also, after a scanning pulse SP was applied to the (3i+2)th gate lines GL2, GL5, ..., the scanning pulse SP is applied to the (3i+3)th gate lines GL3, GL6, ... preceded by a desired line. Furthermore, after a scanning pulse SP was applied to the (3i+3)th gate lines GL3, GL6, ..., the scanning pulse SP is applied to the (3i+1)th gate lines GL1, GL4, ... preceded by a desired line. In other words, a scanning pulse SP is applied to two gate lines GL by utilizing the first to third gate output enable signals GOE1 to GOE3.

If a scanning pulse SP is currently applied to the 31st gate line GL31 and the 62nd gate line GL62, then a picture in the current frame 40 is displayed at the high-order lines of the 31st gate line GL31 in a liquid crystal display panel 44 while a picture in the previous frame 46 is displayed at the low-order lines of the 62nd gate line GL62, as shown in Fig. 10.

On the other hand, a black picture 42 is displayed between the 31st gate line GL31 and the 62nd gate line GL62. In other words, the data driver supplies a picture data D to the data lines DL when a scanning pulse SP is applied to the 31st gate line GL31, and supplies a reset data R to the data lines DL when a scanning pulse SP is applied to the 62nd gate line GL62.

In this case, since the reset pulse R displays a black picture, a picture to be displayed on the liquid crystal display panel 44 is displayed over the black picture. In other words, a picture to be currently displayed is displayed over a picture having previously displayed in the prior art, whereas it is always displayed over the black picture irrespectively of the previous picture in the present invention. Accordingly, it is possible to prevent a motion blur phenomenon caused by an overlapping of a

picture to be currently displayed with a picture having previously displayed.

Furthermore, in the present invention, a capacitor value of the liquid crystal cell Clc in the above-mentioned equation (1) is always fixed. In other words, since a picture to be currently displayed is always displayed over the black picture, a capacitor value of the liquid crystal cell Clc is always fixed to a value when the black picture is displayed. Accordingly, a voltage drop amount ΔV of the data pulse can be forecasted, to thereby compensate for the voltage drop amount ΔV of the data pulse.

Fig. 11 shows driving waveforms of the gate driver according to a second embodiment of the present invention.

Referring to Fig. 11, the gate driver is synchronized with a clock signal to sequentially apply a scanning pulse SP to the (3i+1)th, (3i+2)th and (3i+3)th gate lines GL. When a scanning pulse SP is applied to the (3i+1)th gate lines GL1, GL4, ..., the scanning pulse SP also is applied to the (3i+3)th gate lines GL3, GL6, ... preceded by a desired line. Also, when a scanning pulse SP is applied to the (3i+2)th gate lines GL2, GL5, ..., the scanning pulse SP also is applied to the (3i+1)th gate lines GL1, GL4, ... preceded by a desired line. Furthermore, when a scanning pulse SP is applied to the (3i+3)th gate lines GL3, GL6, ..., the scanning pulse SP also is applied to the (3i+2)th gate lines GL2, GL5, ... preceded by a desired line. In other words, in the second embodiment of the present invention, a scanning pulse SP is applied to two gate lines GL during one period of the clock signal by utilizing the first to third gate output enable signals GOE1 to GOE3.

[Effect of the Invention]

As described above, according to the present invention, two gate lines are alternately scanned in one frame, and a black data is supplied when any one of the two gate lines

is scanned while a picture data is supplied when the remaining gate line is scanned. Accordingly, since a desired picture is displayed over the black picture, it becomes possible to prevent a motion blur phenomenon. Also, it becomes possible to forecast a capacitor value of the liquid crystal cell. A capacitor value of the liquid crystal cell is fixed, so that a voltage drop amount of the data pulse can be forecasted to thereby compensate the voltage drop amount of the data pulse.

Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.